Large Synoptic Survey Telescope Camera System Plan [?]	Document No. **LCA-10098-A** [?] Author(s) S. Herrmann	Status [?] LSST Camera APPROVED Effective Date 17 July 2018
	Subsystem [?] Auxiliary Electronics	

Document Title

Electrical, Electronic, and Electromechanical (EEE) Parts Control Plan

1 Change History Log

Revision	Effective Date	Description of Changes
1.0	24 June 2015	First draft.
A	July 17, 2018	Released per LCN-2144.

2 Contents

3 Introduction

3.1 Purpose

This document describes the LSST Camera electrical, electronic, and electromechanical (EEE) parts program. It summarizes the techniques and methods by which the EEE parts program achieves maximum reliability within cost and schedule constraints. The EEE parts program will ensure that all parts and assemblies used are of the highest level of reliability available consistent with their functional requirements, as well as program cost and schedule constraints. The LSST Camera Part Control Board (PAB) has the primary responsibility of conducting the EEE parts program for the LSST camera

Only parts listed in the LSST camera approved parts list (APL) shall be allowed in the LSST camera. Collaborators can file Nonstandard Parts Approval Request (NSPAR) for approval by the Part Control Board (PAB) during the course of the whole project. Approved parts are then added to the APL.

The purpose of this document is to define criteria for selecting, screening, qualification, and monitoring of EEE parts and assemblies used in the LSST Camera hardware being built by subcontractors, vendors, or collaborators based on the LSST reliability objective.

Should there be a conflict between this document and the LSST requirements (LSE-59, LCA-48) the LSST requirements shall take precedence.

The EEE program will be based on the evaluation of the following three critical reliability factors:

- The materials and processes employed in a device’s manufacture;
- The tests and inspections to which a device is subjected; and
- The electrical and environmental stresses experienced in a device’s application.

The part reliability enhancement, assurance techniques and methods defined herein address five major activities that comprise the LSST Camera electrical, electronic, and electromechanical (EEE) parts program.

These activities are:

- Parts selection
  - LSST camera preferred part list
  - list of applicable part standards
  - Part Assurance Board (PAB) decides on non-standard part approval request (NSPAR) (this usually requires qualification data for the part in question)
  - Part Assurance Board (PAB) decides on screening requirements
- Parts procurement (centralized or distributed - TBD)
- Controlled parts storage (centralized or distributed - TBD)
- Additional part screening performed by collaborators
- Solder process definition (lead free control plan, workmanship standards TBD)
- Screening procedures on complete electronic assemblies

3.2 Scope

This plan establishes the requirements of the LSST camera EEE parts baseline and is based on the requirements specified in LSST LCA XXX and YYYY. It applies to all custom build printed circuit boards inside and outside the cryostat. The following part types shall be subject to LSST camera EEE PAB control:

- Resistors , capacitors, inductors
- Crystals and oscillators
- Discrete semiconductor devices (diodes, transistors, …)
- Microcircuits, hybrid and monolithic, open, hermetic and plastic encapsulated
- Application Specific Integrated Circuits (ASICs),
- Multi-Chip Modules (MCM),
- Heaters, thermo electric coolers
- Wires and cables
- Connectors (board to board, board to cable, cable to cable)
- Fiber optic components
- Printed Circuit Boards and High Density Interconnects
- Motors TBD
- COTS units (like HCUs) TBD

The following definitions are used throughout this document:

- "Shall" defines a requirement that requires a waiver if not performed.
- "Will" defines a function that is expected to be performed during the implementation of the Project's Parts Program, however does not require a waiver when not performed.
- "Should" defines a "best practice" and is strongly recommended but does not require a waiver when not performed.

4 Applicable Documents and Reference Documents (Required)

The following documents of the issue in effect, at the time of the LSST Camera support program, form a part of the requirements of this control plan, to the extent referenced herein. If there is any conflict between this document and the documents listed herein, this document will take precedence.

Ref #	Document Number and Title
	ESA Documents (http://escies.org)
[1]	ECSS-Q-ST-60C-Rev2, "Space product assurance Electrical, electronic and electromechanical (EEE) components"
[2]	ECSS-Q-30-08A, "Components reliability data sources and their use"
[3]	ECSS-Q-ST-30-11C-Rev1, "Derating - EEE components"
[4]	ESCC QPL, "Qualified Parts List"
[5]	ESCC QML, "Qualified Manufacturers List"
[6]	EPPL European Preferred Parts List (includes non-qualified but recommended parts
[7]	STM-281, "Guidelines for creating a LFCP (lead free control plan)"
	NASA Documents
[8]	NASA Policy Directive NPD 8730.2
[9]	NASA EEE-INST-002, "Instructions for EEE Parts Selection, Screening, Qualification, and Derating"
[10]	MSFC-STD-3012 "EEE Parts Management and Control for MSFC Space Flight Hardware"
[11]	JSC SSP 30312 "EEE Parts Management and Implementation Plan for the Space Station Program"
[12]	JSC-66491 "Standard for JSC Lead-Free Control Plans"
[13]	JPL Rules Doc 57732 "Institutional Parts Program Requirements (IPPR) "
[14]	GEIA-STD-0005-1 "Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder"
[15]	GSFC-311- INST- 001 "Goddard Space Flight Center Instructions for EEE Parts Selection, Screening and Qualification"
[16]	GSFC-PPL - 21 "GSFC Preferred Parts List (http://epims.gsfc.nasa.gov) "
[17]	GSFC-S-311-M- 70 "Specification for Destructive Physical Analysis (DPA) "
[18]	GSFC-TR04 -0600 "Plastic Encapsulated Microcircuit Derating, Storage and Qualification Report"
[19]	MIL-STD-883 "Test methods and procedures for Microelectronics"
[20]	MIL-PRF- 19500 Semiconductor Devices, General Specification for"

Ref #	Document Number and Title
[21]	MIL-M- 38510 “Microcircuits, General Specification for”
[22]	MIL-PRF- 38534 “Hybrid Microcircuit, General Specification for”
[23]	MIL-PRF- 38535 “Microcircuits Manufacturing, General Specification for”
[24]	NASA Reference Publication (RP) 1124 “Outgassing Data for Selecting Spacecraft Material”
[25]	NHB 8060.1 “Flammability, Odor and Offgassing Requirements and Test Procedures for Materials in Environments that Support Combustion”
[26]	NASA Parts Selection List (NPSL) ”
[27]	Entire NASA Parts Selection List – http://nepp.nasa.gov/npsl (formerly MIL-STD-975) ”
[28]	433 - SPEC-0001, ” Gamma - Ray Large Area Space Telescope (GLAST) Project Mission System Specification”
	Electronics Industries Association (EIA) Documents
[29]	JESD 22-A102, ”Accelerated Moisture on unbiased Autoclave
[30]	JESD 22-A101, ”STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST
[31]	JESD 22-A104, ”TEMPERATURE CYCLING
[32]	JESD 22-A108, ”TEMPERATURE, BIAS, A ND OPERATING LIFE
[33]	JESD 22-A110, ”HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)
[34]	JESD 22-A113-A, ”PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING
[35]	LAT-MD- 00099- 03, ”LSST Camera EEE Parts Program Control Plan November 2001 7
[36]	JEDEC STANDARD 26 PROPOSED GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS
[37]	IPC/JEDEC J- STD- 020A, ”MOISTURE REFLOW SENSITIVITY CLASSIFICATION
[38]	IPC/JEDEC J- STD- 033, ”STANDARD FOR HANDLING, PACKING, SHIPPING, AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE MOUNT DEVICES
[39]	IPC/JEDEC J- STD- 035, ”ACOUSTIC MICROSCOPY FOR NON -HERMETIC ENCAPSULATED ELECTRONIC COMPONENTS
[40]	ANSI /IPC- SM- 786 , ”RECOMMENDED PROCEDURES FOR HANDLING OF MOISTURE SENSITIVE PLASTIC IC PACKAGES
	American Society for Testing (ASTM) Documents
[41]	ASTM- E - 595, “Standard Test Method for Total Mass Loss and Collected Volatile Condensable Material from Outgassing in a Vacuum Environment”

5 Definitions (Required)

5.1 Acronyms (Required)

Define all acronyms in the document. All Camera documents should include this section.

Table 1: Example Acronyms List

Acronym	Definition
ASIC	Application Specific Integrated Circuit
COTS	Commercial Off-the-Shelf
CSI	Customer Source Inspection
DPA	Destructive Physical Analysis
DSCC	Defense Supply Center Corporation
ESD	Electrostatic Discharge
EEE	Electrical, Electronic, and Electromechanical
ELDRS	Extreme Low Dose Rate Susceptibility
EPPP	Electronic Parts Program Plan
EPQA	Electronic Parts Quality Assurance
ESD	Electrostatic Discharge
FPGA	Field Programmable Gate Arrays
GIDEP	Government Industry Data Exchange Program
HDI	High Density Interconnect
IR	Inspection Report
LET	Linear Energy Transfer
MCM	Multi-Chip Module
MeV	Mega (Million) Electron Volts
MMR	Monthly Management Review
MRB	Material Review Board
MRR	Manufacturing Readiness Review
NSPAR	Non-Standard Parts Approval Request
PAPL	Program Authorized Parts List
PEM	Plastic Encapsulated Microcircuits
PIND	Particle Impact Noise Detection testing
PPE	Parts Program Engineer
PIE	Project Interface Engineer
PPPR	Project Parts Program Requirements
PRB	Parts Review Board
PPBI	Post Programming Burn-In
PPS	Parts Program Specialist
PROM	Programmable Read Only Memories
QA	Quality Assurance
RGA	Residual Gas Analysis
SCD	Source Control Document

5.2 Definitions (As Needed)

In specifications and contractual documents, define terms and phrases that require a particular interpretation. Also define specialized technical terms and phrases that may not be familiar to all readers. Most Camera documents should include this section.

Table 2: Example Definitions

Term	Definition
Packaged Device	A device that has completed the full assembly process including connector installation and package assembly.

Term	Definition
Tested Device	A device that has been tested to meet the EO and mechanical requirements in the Technical Specification.
Science Device	A packaged and tested unit meeting all requirements in the Technical Specification, sections 6.1 and 6.2 (see Ref [2]).

6 Parts Selection and Standardization Requirements

Only parts of acceptable quality, reliability, and contamination compliance, as demonstrated through test and/or analysis that meet or exceed the LSST camera performance and reliability requirements, will be selected for use.

Only parts listed in the LSST camera approved parts list (APL) shall be allowed in the LSST camera. All standard parts are considered to be APL parts even if not explicitly listed there.

Collaborators can file Non-standard Parts Approval Request (NSPAR) for approval by the Part Control Board (PAB) during the course of the whole project. Approved parts are then added to the APL.

6.1 Standard Parts

For the project, standard parts shall be defined as those that meet or exceed any of the following reliability standards:

- NASA EEE-INST-002, Level 1
- MIL-PRF-38534 Class K QML Source
- MIL-PRF-38535 Class V, QML-38535
- MIL-PRF-19500 JANS, QPL-19500
- NASA EEE-INST-002, Level 2,
- MIL-PRF-38534, Class H, QML-38534 (MIL-PRF-38510, Class B
- MIL-PRF-38535, Class Q, QML-38535
- MIL-PRF-19500, JANTXV, QPL-19500
- Military Established Reliability (ER) passive devices, Failure Rate Level S or R

6.2 Non-Standard Parts

Parts not meeting the minimum quality and reliability criteria of standard parts are defined as non-standard parts. Unique, custom parts (e.g., ASICs and Custom Hybrids) are considered non-standard. All non-standard parts shall be upgraded/screened to the LSST requirements as specified on individual NSPAR's (Non-Standard Part Approval Request) by the PAB. This includes assessment of contamination compliance.

6.3 Application Specific Integrated Circuit (ASIC) Requirements

6.3.1 Digital ASIC Test Requirements

Digital logic circuitry in ASICs (including microprocessor, microcontroller and all custom designs) shall be tested to at least 95% stuck-at fault coverage as is defined by MIL-STD-883, Method 5012. In addition, each major functional element of the design shall be tested to at least 90% stuck-at fault coverage.

Quiescent current (all vector Iddq method) tests shall be based on a set of vectors that will toggle 95% of the nodes. In addition, each major functional element of the design shall be tested to at least 90% node toggle coverage.

Additional tests shall be conducted at room temperature and at maximum rated (hot and cold) temperature that include:

- Operating speed (or maximum testable speed) functional test to verify all functions of the design and,
- DC and AC parametric test vectors in compliance with the ASIC specification.

6.3.2 Mixed-signal ASIC Test Requirements

For Mixed-signal ASICs with large monolithic digital elements that amount to more than 10% of the design and more than 500 gates, these digital elements shall meet the requirements in paragraph 2.4.1.

For Mixed-signal ASICs which are predominantly analog circuits with intermingled flip-flops, registers and counters that amount to less than 10% of the overall design complexity and less than 500 gates, these intermingled digital elements are exempt from the requirements in paragraph 2.4.1.

Analog, digital, and mixed signal ASICs shall be modeled or simulated and compared with test data.

Additional tests shall be conducted at room temperature and at maximum rated (hot and cold) temperature3 that include:

- Operating speed (or maximum testable speed) functional test to verify all functions of the design and,
- DC and AC parametric test vectors in compliance with the ASIC specification.

6.4 Custom Hybrid, MCM and HDI Microcircuits

Custom hybrid devices designed and fabricated by non-QML sources shall be in conformance with requirements of Class K reliability level of MIL-PRF-38534. Custom hybrid QML sources shall be in conformance with Class H reliability level of MIL-PRF-38534 with a recommended additional 10-piece Class K element evaluation for each device type. Pre-cap visual inspection and document review (e.g. element evaluation, burn-in data and rework travelers) prior to seal shall be required for all hybrids.

To ensure high yields in small lot production runs, all substrates for use in custom hybrids or MCMs, shall be subjected to MIL-PRF-38534 substrate element evaluation.

The PAB will identify in-process inspection points commensurate with Project requirements and will be called out in the travelers and inspected by QA.

6.5 Wet electrolytic capacitors

There shall be no wet electrolytic capacitors used.

6.6 In cryostat additional qualification for contamination compliance

All parts which will go into the LSST camera cryostat shall be qualified for their contamination compliance as described in the contamination control plan LCA-279.

7 Assembly and Solder processes.

7.1 Printed circuit board terminations for soldering and solder process

Printed circuit boards will be terminated with ENEPIG suitable for RoHS compatible solder process using SAC405.

7.2 Assembly and soldering

Assembly shall only be performed in approved workshops. TBD

8 Assembly qualification and screening requirements

8.1 Qualification

Designs intended for production shall be qualified to demonstrate that the design is capable to fulfill the LSST requirements. The qualification results shall be shown at the MRR and submitted to the PAB. The following qualification tests shall be performed at a minimum.

8.1.1 Assembly thermal cycle qualification

A sample number of fully representative assemblies of MRR ready designs shall be thermal cycled 1000 times from -30 to 85C (ramp rate of 10-20C/min and a 10 min dwell time) followed by optical inspection and functional test.

(i.e. see JESD22-A104-B as guide)

8.1.2 Contamination compliance qualification

A sample number of fully representative assemblies of MRR ready designs shall be evaluated for their contamination compliance according to LCA-279

8.2 Screening

All assemblies which will be used for the LSST camera shall be screened according to the following tests.

8.2.1 Assembly thermal cycle screening

All assemblies shall be thermal cycled 10 times from -30 to 85C (ramp rate of 10-20C/min and a 10 min dwell time) followed by optical inspection and functional test.

(i.e. see JESD22-A104-B as guide)

8.2.2 Assembly burn-in screening

All assemblies shall be burned in at +65C for at least 72h followed by a functional test. Evaluation of the change of performance parameter before and after the burn in is recommended.

8.2.3 Assembly contamination screening

All assemblies which go into the cryostat vacuum volume shall be evaluated for their contamination compliance according to LCA-279 prior to integration.

9 Management

9.1 Part Assurance Board

The LSST camera Part Assurance Board (PAB) will be responsible for the management of the EEE Parts Program. All EEE parts used on the project shall be reviewed by the PAB. The review results are to be documented. The PAB shall generate a Project Parts List for tracking potential parts application issues and stress. The Project shall keep the parts list current and has it reviewed for risk assessment prior to build and periodically throughout the development process. The PAB will provide a written risk-rating summary to the project based on the review results. The PAB will decide on approval of risk waivers for parts after review together with LSST management. The LSST Camera ASICs will go through package level testing and screening/qualification process. LSST Camera PAB will also review and accept the screening/qualification plans for the commercial-off-the shelf (COTS) PEMS for use in the LSST Camera.

9.1.1 Application Specific Integrated Circuit (ASIC) Requirements

The ASIC Parts Specialist shall be a member of the design team and attend ASIC Design team meetings. ASIC design guidelines to monitor the design and test vector generation will be documented and reviewed by the ASIC Parts Specialist. All ASIC developments for the project shall have Preliminary Design Reviews, Critical Design Reviews, Manufacturing Readiness Review, and Monthly Management Reviews to monitor technical, budget, and schedule progress. The Parts Interface Engineer and Parts Specialists will participate in all reviews.

The design reviews will address as a minimum, derating requirements, parts screening and qualification, temperature effects evaluation, verification of controlled engineering materials, processes and other design analysis as applicable to the LSST camera requirements.

9.1.2 Custom Hybrid, MCM and HDI Microcircuits

The Hybrid Parts Specialist shall be a member of the design team and attend Hybrid Design team meetings to monitor the design and test methodology. All projects requiring hybrid microcircuits shall have Preliminary Design Reviews, Critical Design Reviews, Manufacturing Readiness Review, Peer Reviews and Monthly Management Reviews7. The Parts Interface Engineer and Parts Specialists will participate in all reviews. The design reviews will address, as a minimum; derating requirements, element evaluation and quality levels, outgassing effects evaluation, verification and control of materials, processes, thermal and other design analysis as applicable to mission requirements.

9.2 Non-Standard Part Approval

In order for non-standard parts to obtain approval for use, a NSPAR form (attachment 1) shall be submitted with full supporting data including

- datasheet(s)
- documentation for the intended operating conditions
- procurement source

- screening specifications
- reliability test data/analysis
- outgassing test data/analysis

NSPAR's shall be reviewed and approved by the PAB.

9.2.1 Parts List Review

A list of part types considered by the design organization to be design candidates should be submitted in Excel format. The submittal of the preliminary design list will be at least 30 days prior to subsystem FDR. A final "As-designed" list shall be submitted at a minimum of 30 days prior to MRR of each subsystem. All additions or modifications will be highlighted and submitted within one month of the change.

The parts lists should include:

- part number
- value/tolerance/rating
- part specification/source control drawing number
- generic part number
- part description (e.g., ceramic capacitor, or quad nor gate)
- proposed part manufacturer
- the review and approval status for nonstandard parts
- the review and approval status of any waivers
- an estimate of the quantities to be used
- application usage notes that can aid the PAB in reviewing parts

9.2.2 As-Built Parts List

The PAB will review the As-Built Parts List for risk assessment. In addition to the information required in the parts lists, the as-built parts list should include for each different part the following:

- actual part marking
- part number
- manufacturer
- lot date code
- serial number (for serialized parts)
- procurement specification number

9.2.3 Non-Compliant Parts

Whenever a standard or non-standard part fails to comply with the requirements established herein, an Inspection Report (IR) shall be generated.

9.3 Parts Acquisition

9.3.1 Parts Procurement

Parts for LSST camera equipment shall be procured directly from the approved part manufacturers or authorized distributor when traceability to the manufacturer can be established. Purchase orders and/or purchase requisitions shall not contain exceptions to referenced specifications or requirements unless approved via the NSPAR.

9.3.2 Traceability

All parts purchased under this program shall be traceable to a specific manufacturer, part number, and lot number or lot date code. In addition, parts requiring serial numbers will have traceability to test data associated with the same lot.

9.3.3 Parts Data Requirements and Data Retention

The manufacturer's or vendor's certificate of conformance for each electronic part lot shall be obtained by the procuring activity and retained for a period of launch plus three years or as directed by the Project. The parametric data will be traceable to each serialized part. All variables and attributes data generated in compliance with the specification will be delivered to the procuring activity. The data shall be reviewed by the procuring activity for technical acceptability and completeness. The read and record data may be required when the project needs to establish worst case circuit analysis parametric data points. This will be included in the parts procurement as requested by the project. All test and evaluation data will be submitted to the PIE for review (electronic format is preferred).

9.3.4 Customer Source Inspection (CSI)

When parts are procured pre-seal visual inspection shall be performed by LSST Procurement Quality Assurance organization on all packaged ASICs, hybrid microcircuits, MCMs, crystal oscillators, and relays by the procuring agency

9.3.5 Electronic Parts Quality Assurance (EPQA)

All incoming LSST camera parts shall be inspected by EPQA prior to final storage.

All piece parts requiring upgrades, screenings or testing shall be inspected by EPQA prior to shipping to the vendor and shall be re-inspected by EPQA upon their return.

9.4 Electronic Parts Application and Derating

9.4.1 Parts Derating

Each part used in the LSST camera will be applied in a manner such that the temperatures experienced and electrical stresses produced when it is operating do not exceed the derating criteria defined in the derating appendix.

9.4.2 Handling / Storage / Electrostatic Discharge (ESD) Control Requirements

ESD damage or degradation may occur in static-sensitive electronic parts during handling of the parts from procurement through incoming inspection, testing, screening, storing and final assembly/test. To protect static-sensitive parts from ESD, handling of parts shall be controlled by the requirements of JPL D-1348, or equivalent.

9.4.3 Failure Analysis

Failure analysis shall be performed for all part failures that occur during screening (for custom devices and parts that require upscreening) and subsequent. The only exceptions are parts damaged by human error (e.g., improper installation). Analysis shall be carried to the point that lot dependency of the failure mode can be determined. Failure analysis reports will be written to document the analysis approach, the determined failure mode and mechanism (i.e., cause) responsible for the failure, and the corrective actions required to prevent recurrence of the failure.

10 Appendixes

10.1 Appendix A: Derating Guidelines for Hermetic Devices

Appendix A available separately.

10.2 Appendix B: Derating Guidelines for PEM Microcircuits

Appendix B available separately.

10.3 Appendix C: Stress Analysis Worksheets

Appendix C available separately.

10.4 Appendix D: Typical PAB Approval Request Form

Appendix D available separately.

APPENDIX A

DERATING GUIDELINES FOR HERMETIC DEVICES

(for more details, refer to the PPL-21 web-site http://nepp.nasa.gov)

Capacitors

Voltage derating is accomplished by multiplying the maximum operating voltage by the appropriate derating factor appearing in the table below.

Type	Military Style	Voltage Derating Factor	Maximum Ambient Temperature
Ceramic	CCR. CKS, CKR, CDR, DSCC-DWG-87106, PS	0.6	110ºC
Glass	CYR	0.5	110ºC
Plastic Film	CRH, CHS	0.6	85ºC
Tantalum, Foil	CLR25, CLR27, CLR35, CLR37	0.5	70ºC
Tantalum, Wet Slug	CLR79, CLR81, CLR90, CLR91	0.6 0.4	70ºC 110ºC
Tantalum, Solid	CSR, CSS, CWR	0.5 0.3	70ºC 110ºC

Circuit Breakers

Circuit breaker contacts are derated by multiplying the maximum rated contact current (resistive) by the appropriate contact-derating factor listed below.

Contact Application	Contact Current Derating Factor	Maximum Ambient Temperature
Resistive	0.75	20ºC below maximum rated temperature
Capacitive	0.75	
Inductor	0.40	
Motor	0.20	
Filament	0.10	

Fuses

Fuses are derated by multiplying the rated amperes by the appropriate derating factor listed below.

Fuse Current Rating (Amperes) @ 25ºC	Current Derating Factor	Derated Fuse Current (A)	Temperature Derating Factor	Remarks
2 – 15	50%	1 – 7.5		

1, 1 ½	45%	0.45, 0.675	Apply additional derating of 0.5%/°C for an increase in the temperature of fuse body is above 25°C	
¾	40%	0.3		
½	40%	0.2		The flight use of fuses rated ½ A or less requires application approval by the parts specialist and/or project office
3/8	35%	0.13125		
¼	30%	0.075		
1/8	25%	0.03125		

Connectors

Connectors of all types/styles are derated by limiting the temperature seen by the dielectric insert due to ambient temperature and the effects of resistive heating.

Operating Voltage Derating	25% of the rated dielectric withstanding voltage at sea level
Temperature Derating of the Dielectric Insert	Temp. Rating ≥ Ta + Toh + 50°C

Notes: Ta = Ambient Temperature, Toh = Ohmic Heating Temperature

Crystals:

Rated Drive Level 50% of the rated value.

Operating Temperature 10°C higher than the minimum specified value

10°C lower than the maximum specified value

Frequency Shift Allow for 4 times the frequency shift in the procurement specifications

Crystal Oscillators:

Crystal oscillators are hybrid parts that contain a number of microcircuits and ot her electronic components. Crystal oscillators should be derated at the individual component level. Crystal current should be derated to 50% of the rated value. In cases where start-up time is critical, 75% of the rated value should be used. Some of the components used in the crystal oscillator may degrade in radiation environment. The crystal oscillator parameters that may get affected include current, frequency and frequency shift. Consult the project radiation specialist to evaluate the effect of radiation environment on the individual components and hence on the crystal oscillator.

Filters

Derating is accomplished by multiplying the current and voltage by the appropriate derating factor appearing in the chart below.

Class	Stress Parameter (Note 1)	Derating Factor
ALL	Rated Current	0.50
	Rated Voltage	0.50
	Maximum Ambient Temperature	85ºC, or 30ºC less than maximum rated temperature, whichever is less

Note 1: Applies to rated operating current or wattage, not the absolute maximum

Inductors and Coils

Inductors are derated by reducing the maximum operating temperature based on the insulation class used and reducing the operating voltage. See notes below.

Insulation Class		Maximum Operating Parameters		
MIL-PRF-39010	MIL-PRF-15305	Rated Operating Temperature	Derated Operating Temperature	Operating Voltage
-	O	+85ºC	+65ºC	Derate to 50% of the rated dielectric withstanding voltage
A	A	+105ºC	+85ºC	
B	B	+125ºC	105ºC	
F	-	+150ºC	130ºC	

Notes:

1. Maximum operating temperature equals ambient temperature plus temperature rise, plus 10ºC (allowance for hot spot). Compute temperature rises as follows:

Temperature rise test (per MIL-T-27, 4.8.12) Temp. Rise (ºC)

$= (R - r)/r \times (t + 234.5ºC) - (T - t)$

- R = winding resistance at elevated temperature
- r = winding resistance at ambient temperature
- t = specified initial ambient temperature (ºC)
- T = maximum ambient temperature (ºC) at time of power shutoff.

T should not differ from t by more than 5ºC.

2. The insulation classes of MIL-style inductive parts generally have maximum operating temperature rating based on a life expectancy of 10,000 hours. The maximum operating temperatures in this table are selected to extend the life expectancy to 50,000 hours.

3. Custom made inductive devices should be evaluated on a materials basis to determine the maximum operating temperature. Devices with temperature ratings different from the military insulation classes should be derated to 0.75 times maximum operating temperature.

Relays

Subtable T (Ambient Operating Temperature)		Subtable R (Cycle Rate)		Subtable L (Load)	
Temperature Range	Factor	Cycle Rate per Hour	Factor	Load Application	Factor
+85°C to +125°C	0.7	>10	0.85	Make, break and/or carry loads with an on-time duration of 0 to 500ms. Off time is equal to or greater than n time.	1
+40°C to +84°C	0.85	1 to 10	0.90	Carry-only loads. Relay does not make or break the load. Maximum on time is 5 minutes. Off time is equal to or greater than on time.	1.5
-20°C to +39°C	0.9	<1	0.85	All other load conditions	0.8
-65°C to -21°C	0.85				

Notes:

1. DO NOT derate coil voltage or current. Operating a relay at less than nominal coil rating can result in either switching failures or increased switching times. The latter condition induces contact damage because of the longer arcing time, thus reducing relay capacity.
2. For additional information see PPL-21.

Resistors

Style	Description	Derating Factors (1) Power	Derating Factors (2) Voltage	Derating Temperatures T1	Derating Temperatures T2	Specification Maximum Storage Temperature T3
G311P672	Fixed, High Voltage	0.6	0.8	70	94	110
G311P683	Fixed, Precision, High Voltage	0.6	0.8	125	185	225
G311P742	Fixed, Low TC, Precision	0.6	0.8	125	155	175
RBR	Fixed, Wirewound (accurate), Established Reliability					
1%		0.6	0.8	125	137	145
0.5%		0.35	0.8	125	132	145
0.1%		0.25	0.8	125	130	145

RWR	Fixed, Wirewound (power type), Established Reliability	0.6	0.8	25	160	250
RCR (3)	Fixed, Composition (Insulated), Established Reliability	0.6	0.8	70	(4)	(4)
RER	Fixed, Wirewound (power type), chassis mounted, Established Reliability	0.6	0.8	25	160	250
RTR	Variable, Wirewound (lead screw actuated), Established Reliability	0.6	0.8	85	124	150
RLR	Fixed, Film (insulated), Established Reliability					
100ppm		0.6	0.8	70	118	150
350ppm		0.6	0.8	70	103	125
RNC, RNR, RNN	Fixed, Film, Established Reliability	0.6	0.8	125	155	175
RM	Fixed, Film, Chip, Established Reliability	0.6	0.8	70	118	150
RZ	Fixed, Film, Networks	0.6	0.8	70	103	125
Others	Various	0.5	0.8	(5)	(5)	(5)

Notes:

1. For the ambient temperatures ≤T1, compute the resistor's derated power level by multiplying its nominal power rating by the appropriate derating factor. If the resistor is operated above T1, derate linearly from the T1 power level to the zero power level at T2. Exposing the resistor to temperatures exceeding T3, even under no load conditions, may result in permanent degradation. The graphs that follow visually depict the power derating profiles described in tabular form above for the various resistor styles.
2. The maximum applied voltage should not exceed the lesser of the following: (1) 80% of the specified maximum voltage rating or (2) the square root of: the derated power (Watts) multiplied by the resistance of that portion of the element actually active in the circuit.

This voltage derating applies to dc and regular ac waveform applications. For pulse and other irregular waveform applications, consult MIL-HDBK-978 or the manufacturer.

3. The last known source for military grade, carbon composition resistors ceased production in 1996. Derating guidelines are provided for projects using residual stock. NASA Parts Advisory NA-033 dated July3, 1996 discusses this diminishing source topic in detail. Consult the EPIMS (http://misspiggy.gsfc.nasa.gov) database for details of this advisory.
4. Determine the maximum storage temperature (T3) from the applicable detail specification. Compute the derated zero power temperature (T2) from the following formula:

T2 = D(T3 – T1) + T1, where:

T2 = Derated zero power temperature

D = Derating Factor

T3 = Maximum storage temperature from applicable specification sheet

T1 = Rated power temperature.

5. Determine the rated power, the rated power temperature (T1), and the maximum storage temperature (T3) from the manufacturer's specification. Calculate the derated zero power temperature (T2) as per the previous note.

Thermistors

Positive Temperature Coefficient (PTC) thermistors are generally operated in the self-heat mode. Derate to 50 percent of the rated power, or as required by the detail specification.

Negative Temperature Coefficient (NTC) thermistors operated in the self-heat mode should be derated in accordance with the figure provided in PPL-21. Such parts should be derated to a power level causing maximum increase of 50 times the dissipation constant, or a maximum part temperature of 100°C, whichever is less.

Transformers

Transformers are derated by limiting the maximum operating temperature based on the insulation class used, and limiting the rated operating voltage to 50% of its maximum.

Insulation Class		Derated Maximum Operating Parameters	
MIL-PRF-27	MIL-PRF-21038	Temperature	Dielectric Withstanding Voltage
Q(+85ºC)	Q(+85ºC)	+65ºC	50% of maximum rated operating voltage
R(+1055ºC)	R(+105ºC)	+85ºC	
S(+130ºC)	S(+130ºC)	105ºC	
V(+155ºC)	T(+155ºC)	130ºC	
T(+170ºC)	U(+170ºC)	155ºC	

Notes:

1. Maximum operating temperature equals ambient temperature plus temperature rise, plus 10ºC (allowance for hot spot). Compute temperature rises as follows:

Temperature rise test (per MIL-T-27, 4.8.12) Temp. Rise (ºC)

$= (R - r)/r \times (t + 234.5ºC) - (T - t)$

- R = winding resistance at elevated temperature
- r = winding resistance at ambient temperature
- t = specified initial ambient temperature (ºC)

- T = maximum ambient temperature (ºC) at time of power shutoff.

T should not differ from t by more than 5ºC.

2. The insulation classes of MIL-style inductive parts generally have maximum operating temperature rating based on a life expectancy of 10,000 hours. The maximum operating temperatures in this table are selected to extend the life expectancy to 50,000 hours.
3. Custom made inductive devices should be evaluated on a materials basis and stressed at levels below the maximum operating temperature for the materials used. Devices having maximum rated operating temperatures in the range from +85°C to +130°C, should be derated as follows: maximum operating temperature (°C) equals 0.75 times maximum rated operating temperature. For devices with maximum rated temperatures outside this temperature range, consult the project parts engineer for temperature derating recommendations.

Wire and Cable

Wire Size (AWG)	Derated Current (Amperes)	
	Single Wire	Bundled Wire or Cable
30	1.3	0.7
28	1.8	1.0
26	2.5	1.4
24	3.3	2.0
22	4.5	2.5
20	6.5	3.7
18	9.2	5.0
16	13.0	6.5
14	19.0	8.5
12	25.0	11.5
10	33.0	16.5
8	44.0	23.0
6	60.0	30.0
4	81.0	40.0
2	108.0	50.0
0	147.0	75.0
00	169.0	87.5

Notes:

1. Derated current ratings are based on an ambient temperature of 70°C or less in a hard vacuum of 10^-6 torr.
2. The derated current ratings are for 200°C rated wire, such as Teflon™ insulated (Type PTFE) wire, in a hard vacuum of 10^-6 torr.
   a. For 150°C wires, use 80% of the value shown above.
   b. For 135°C wires, use 70% of the value shown above.
   c. For 105°C wires, use 50% of the value shown above.
3. The current rating for bundles or cables are base on bundles of 15 or more wires. For additional information see PPL-21.

Diodes

Derating is accomplished by multiplying the critical stress parameter by the appropriate derating factor in the chart below:

Diode Type	Critical Stress Parameter	Derating	Maximum Junction Temperature
General Purpose, Rectifier, Switching, Pin/Schottky, and Thyristors	Peak Inverse Voltage	0.70	125°C, or 40°C below the manufacturer's Maximum rating, whichever is lower
	Surge Current	0.50	
	Forward Current	0.50	
Varactor	Power	0.50	
	Reverse Voltage	0.75	
	Forward Current	0.75	
Voltage Regulator	Power	0.50	
	Zener Current	0.5(I-max + I-nom)	
Voltage Reference	Zener Current	N/A (1)	
Zener Voltage Regulator	Power Dissipation	0.50	
Bi-directional Voltage Suppressor	Power Dissipation	0.50	
FET Current Regulator	Peak Operating Voltage	0.80	
Microwave Diodes	Power Dissipation	0.50	
	Reverse Voltage	0.75	

Note:

Operate at the manufacturers specified Zener current to optimize temperature compensation. For additional information see PPL-21.

Transistors

Derating of transistors is accomplished by multiplying the appropriate stress parameter by its derating factor. Junction temperature must also be calculated and maintained below 125°C or 40°C below the manufacturer's maximum rating, whichever is lower.

Transistor Type	Critical Stress Parameter	Derating Factor	Maximum Junction/Channel Temperature
BIPOLAR			125°C, or 40°C below the manufacturer's Maximum rating, whichever is lower
General purpose, switching, and power	Power	0.50	
	Current	0.75	
	Voltage	0.75 (1)	
FIELD EFFECT			
JFET	Power	0.50	
	Current	0.75	
	Voltage	0.75 (1)	
MOSFET (2)	Power	0.50	
	Current	0.75	
	Voltage (V -ds)	0.75 (1)	
	Voltage (V -fgs)	0.60 (1)	
RF/MICROWAVE			
Silicon GaAs	Power	0.50	
	Current	0.75	
	Voltage	0.75 (1)	

Notes:

1. Worst-case combination of DC, AC, and transient voltages should be no greater than the derated limit.
2. Power MOSFET devices under certain conditions are very susceptible to catastrophic failure mechanisms, specifically Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR), resulting from heavy ion impact. It may be necessary to derate the drain to source voltage (V-ds) and gate to source voltage (V -gs) to 30 – 50 % og the maximum, depending upon the device type, the manufacturer, etc. Consult the applicable parts/radiation specialist for further information and applicable derating guidelines.
3. For additional information see PPL-21.

Digital Microcircuits

Derating of digital microcircuits is accomplished by multiplying the parameter by the appropriate derating factor in the chart below:

Critical Stress Parameters	Bipolar Logic	CMOS Logic		Line Drivers/ Receivers	LSI/VLSI		ASIC - Digital and Mixed Signal
		4000 A/B	Other (3)		Biploar	CMOS	
Absolute Maximum Supply Voltage (1)	(2)	0.70	0.80	0.75	(2)	(2)	(2)
Input Voltage	Under no circumstances should input voltage be allowed to exceed the supply voltage. Logic noise-margin levels should be derated by a factor of 0.80.						
Open Collector/Drain DC Output Voltage	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Operating AC/DC Output Current or Fanout	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Power Dissipation	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Maximum Junction Temperature	100°C, or 40°C below the manufacturer's Maximum rating, whichever is lower						

Notes:

1. For those technologies where no supply voltage derating is specified, in no case shall the device maximum operating supply voltage be exceeded.
2. Use Manufacturer's recommended operating voltages.
3. Includes high speed (HCS/HCTS) and advanced (ACS/ACTS/AC/ACT)

Further derating may be required for radiation induced degradation. Consult the project radiation specialist for derating guidelines, which account for radiation induced degradation in parts over the lifetime of each mission.

Linear Microcircuits

Derating of linear microcircuits is accomplished by multiplying the parameter by the appropriate derating factor in the chart below:

Critical Stress	Comparators	Sense	Operational	Other	Voltage	Analog	A/D and D/A

Parameter		Amplifiers	/ Differential Amplifiers	Amplifiers (1)	Regulators	Switches	Converters
Absolute Maximum Supply Voltage (2)	0.80	0.80	0.80	0.80		0.80	0.80
Differential Input Voltage (4)	0.70	0.70	0.70	0.70			
Single-Ended DC Input Voltage (4)					0.80	0.80	0.80
Open Collector/Drain DC Output Voltage	0.75	0.75					
Operating AC or DC Output Current	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Maximum Short Circuit Output Current	0.80	0.80	0.80	0.80	0.80		
Power Dissipation	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Maximum Junction Temperature	100°C, or 40°C below the manufacturer's Maximum rating, whichever is lower						

Notes:

1. Other amplifiers include current, voltage follower, instrumentation, video and sample and hold.
2. For devices with maximum ratings greater than 10V, derate by at least 2 V below the absolute maximum voltage rating of each rail.
3. V-in – V-out should be derated to 0.80.
4. Under no circumstances should the input voltage be allowed to exceed the supply voltage.

Further derating may be required for radiation induced degradation. Consult the project radiation specialist for derating guidelines, which account for radiation induced degradation in parts over the lifetime of each mission.

Optoelectronic Devices

Derating of transistors is accomplished by multiplying the appropriate stress parameter by its derating factor. Junction temperature must also be calculated and maintained below 100°C or 40°C below the manufacturer's maximum rating, whichever is lower.

Device Type	Critical Stress Parameter	Derating Factor	Maximum Junction/Channel Temperature
Light Emitting Diodes	Power	0.50	
	Current	0.75	

	Voltage	0.75	Maximum junction temperature should be limited to 100°C or 40°C below the manufacturer's maximum rating, whichever is lower.
Photo Diodes Photo Transistors	Power Current Voltage	0.50 0.75 0.75	
Optocouplers (1) (2)	Power Current Voltage	0.50 0.75 0.75	

Notes:

1. For optimum coupling efficiency, use manufacturers recommended operating conditions.
2. Recent experiences have indicated that optocouplers, in general, are usually sensitive to Single-Event transients. Consult with an appropriate specialist prior to selecting optocouplers for flight applications.

Hybrids and Multi Chip Modules (MCMs)

Hybrids make an integral use of chips and discrete parts on a common substrate in a single package to meet the need for unique circuit requirements, often available as an individual microcircuits. On the other hand, the MCM is a chip-only technology with the substrate being an integral part of the product design, not simply a component carrier. The dice are mounted on or embedded in a multilayered substrate that is contained in a protective case that may be hermetic sealed or plastic encapsulated.

Normally the hybrid and MCM packages provide an inherent space saving advantage, however, there are some potentially adverse effects of high-density packaging:

a) Tight/close physical proximity – reduces isolation reduction, resulting in cross-talk

b) Concentrated areas of power dissipation – makes cooling more difficult, effecting reliability and performance.

c) Dissimilar adjacent materials/metals – reduces reliability under temperature extremes (TCE problems) and increases corrosion possibilities.

The failure mechanisms found in microcircuits and passive components, from electrical aging, electrical and mechanical wear out, and radiation, are also found in Hybrids and MCMs. Also, the Hybrid/MCM parts package has a significant effect on the part's life. Packages that dissipate heat effectively and/or protect the internal circuitry from the environment last longer.

APPENDIX B

DERATING GUIDELINES
FOR
PEM MICROCIRCUITS

Type			Environment	
Digital	Package	Derating Parameter	Protected	Normal
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	90%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	90%
		Output Current	90%	80%
		Fanout	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 1. Digital MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	Package	Derating Parameter	Protected	Normal
MOS	Plastic 1/	Supply Voltage	/3	/3
		Input Voltage	80%	70%
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	90%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Input Voltage	60%	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Input Voltage	80%	70%
		Frequency	100%	90%
		Output Current	90%	80%
		Fanout	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Input Voltage	60%	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 2. Linear MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	Package	Derating Parameter	Protected	Normal
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	85%
		Junction Temperature	85°C	75°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	80%	90%
		Output Current	75%	80%
		Fanout	75%	80%
		Junction Temperature	85°C	75°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 3. Microprocessor MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	Package	Derating Parameter	Protected	Normal
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	90%
		Output Current	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	95%
		Output Current	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Junction Temperature	70°C	

Table 4. Microcircuit Memory MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
GaAs	Package	Derating Parameter	Protected	Normal
Digital	Plastic 1/	Channel Temperature	125°C	90°C
	Plastic 2/	Channel Temperature	90°C	

Table 5. Digital MOS and Bipolar Microcircuit Derating Guidelines

Notes for Tables 1-5

Environmental Categories:

Protected Environment – applicable for parts employed according to the following conditions:

a. Used in readily accessible maintenance applications.
b. Used in a controlled environment.
c. Not used in an application with shock, vibration, pressure or moisture.
d. Not stored for later use.
e. With an application life span of up to 5 years.

Normal Environment – applicable for parts employed according to the following conditions:

a. used in inhabited applications

b. Used in applications usually accessible for maintenance or replacement.
c. Used in uncontrolled, but not extreme, temperature environment with a temperature range of -40°C to +85°C.
d. Can be stored for later usage (not exceed 10 years)
e. With an application life span of 5 to 10 years

1/ Plastic packaged microcircuit with heat dissipation mechanisms (e.g. thermal fillers, thermal conductivity plate or a type of metal substrate) built in.

2/ Low – power plastic packaged microcircuits with no heat dissipation mechanism other than through the leads.

3/ The supply voltage must be kept within the microcircuit specification sheets minimum and maximum limit.

APPENDIX C

STRESS ANALYSIS WORKSHEETS

System	Schematic Title:	Drawing No.
	NEXT ASSY. TITLE:	DRAWING NO.

Ref. Des. (Type)	Const-Ruction / Resistive Element	Package Type	Vendor	Procur. Part No.	Norm Resist	Mfg Tol	Ta 1/	Voltage		Power Dissipation			Percent Power Rated	Percent Voltage Rated	Wave Form (dc, sine, pulse, etc)	REMARKS
								Norm Rated	Actual	Rated 25ºC	Rated Max Amp	Actual				
					W	%	ºC	V	V	mW	mW	mW	%	V		
	REPORT NUM. REV DATE				PREPARED BY: DATE					APPROVED BY DATE			SHEET			
	OF															

TABLE 1: EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR RESISTORS
NOTES:
1/ AMBIENT TEMPERATURE

System						Schematic Title:							Drawing No.			
						NEXT ASSY. TITLE:							DRAWING NO.			
Ref. Des. #	Const. Dielec-tric	Cap Type	Vendor	Procur Doc	Part Amb. Temp	Mfg Tol	Cap Value	VOLTAGE					Percent Power Rated	Percent Voltage Rated	Wave Form (dc, sine, pulse, etc)	REMARKS
								Rated Td 1/	DC	FREQ	PULSE PEAK	REP RATE				
					ºC	%		V	VDC	KHz	V	Ms	%	V		
	REPORT NUM.		REV	DATE	PREPARED BY:		DATE		APPROVED BY			DATE	SHEET _____ OF _____			

TABLE 2. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR CAPACITORS

NOTES:

1/ MAXIMUM DERATING TEMPERATURE

SYSTEM								SCHEMATIC TITLE:												DRAWING NO.						
								NEXT ASSY. TITLE:												DRAWING NO.						
Ref Des #	Ven -d Part #	Ven -d	Pro- c Doc	Type GP, power Etc.	Part Amb. Temp.		Contact Arrange- ment	Contact Loading								Coil Voltage								% Cont Power Rating
								Cont- act	Power		Current		Load	Max.		Pickup		Dropout							
					Norm Rated	act			Norm rated	act	Rated	act	Res/ ind cap	Norm rated	act	Rated	act	Norm rated	act							
					°C	°C			mW	mW	mA	mA		mV	mV	mV	mV	mV	mV							
REPORT NUM.		REV	DATE	PREPARED BY:				DATE	APPROVED BY				DATE	SHEET _____ OF _____											

TABLE 3. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR RELAYS

System						Schematic Title:							Drawing No.			
						NEXT ASSY. TITLE:							DRAWING NO.			
Ref. Des. #	Vendor Part #	Vendor	Proc. Part No	Type SI GE	Max Amb Temp	Peak Inverse Voltage		Forward Current		Voltage			Percent Current Rating	Percent PIV Rating	Tj	REMARKS
						Max Rated	Actual	Max Rated	Actual	Rated 25ºC	Rated Max Amp	Actual				
						V	V	mA	mA	V	V	V	%	%	ºC	
REPORT NUM.		REV	DATE	PREPARED BY:		DATE		APPROVED BY		DATE			SHEET _____ OF _____			

TABLE 4. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR ZENER DIODES

System						Schematic Title:							Drawing No.		
						NEXT ASSY. TITLE:							DRAWING NO.		
Ref. Des. #	Vendor Part #	Vendor	Proc. Part No	Type SI GE	Max Amb Temp	Peak Inverse Voltage		Forward Current		Power Dissipation			Percent Current Rating	Percent PIV Rating	REMARKS
						Max Rated	Actual	Max Rated	Actual	Rated 25ºC	Rated Max Amp	Actual			
						V	V	A	A	mW	mW	mW	%	%	
REPORT NUM.		REV	DATE	PREPARED BY:		DATE		APPROVED BY		DATE			SHEET _____ OF _____		

TABLE 5. EXAMPLE PART USAGE AND APPLIED STRESS CHART FOR GENERAL PURPOSE AND POWER RECTIFIER DIODES

System					Schematic Title:											Drawing No.						
					NEXT ASSY. TITLE:											DRAWING NO.						
Ref. Des .#	Vend Part #	Vend	Proc Part No	Part amb temp	Power Dissipation			Voltage						Current			% outp. rating	% supp rating	% curr. rating	% Ic rating	Q Res	T
					Rated		Act	Input		Output		Supply		Collector		% inp. rat-ing						
					@ 25°C	@ Td		rated	act	rated	act	rated	act	rated	act							
				°C	mW	mW	mW	V	V	V	V	V	V	mA	mA	%	%	%	%	%	°C/W	
REPORT NUM. REV DATE					PREPARED BY: DATE							APPROVED BY DATE					SHEET _____ OF _____					

TABLE 6. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR LINEAR MICROCIRCUITS

APPENDIX D:

TYPICAL PAB PART APPROVAL REQUEST FORM

LSST Camera PAB PART APPROVAL REQUEST			
1. Contract Number:	2a. REQUEST Number:		
3. Project Name:		2b. Resubmittal: ☐	
4a. Contractor:			
4b. Subcontractor, vendor, or collaborator:			
5. System & Component:			
6. Part Name:			
7. Part Number:	8. Commercial Part Number:		
9. Part Manufacturer:		FSCM:	
10. Procurement Spec.:	Revision		
11. Screening Spec.:	Revision		
12. Describe Critical Parameters:			
13. Justification for use of Requested Part:			
14. Approval Signatures	Title	Date	
Requested By:			
Reviewed By:			
Approved By:			

INSTRUCTIONS FOR ENTERING DATA ON PAB APPROVAL PARTS APPROVAL REQUEST FORMS

Block 1 - Enter the prime contract number

Block 2a - Enter the serial number to each REQUEST

Block 2b - If this REQUEST is being resubmitted as a result of prior disapproval, check this block.

Block 3 - Enter the Full Project Name

Block 4a - Enter the name of the prime contractor

Block 4b. - Enter the name of the subcontractor, vendor, or collaborator, if applicable

Block 5 - Enter the name of the system and component (BOX) in full for spacecraft systems.

- Enter the name of the experiment or instrument for payload items.

Block 6 - Enter in full, the name of the part; i.e., capacitor, resistor. (use listing in the GSFC preferred parts list PPL-21 as a guide). Multiple parts listings on a s ingle REQUEST are not permitted.

Block 7 - Enter the part number, which uniquely identifies the part. If it is a mil part, enter the mil part number. If it is procured to a source control drawing (SCD), enter the SCD number and dash number associated with the source used. Otherwise use the commercial designation.

Block 8 - Enter the commercial number for the parts.

Block 9 - Enter in full, the name and location of the manufacturer of the part or device and/or the FSCM number. For non-standard MIL-Spec parts, the designation QPL may be used on lieu of manufacturer's identification if the actual source is not known. Multiple source listings may appear on a single request form.

Block 10 -Enter the procurement specification and appropriate revision letter to which the part or device is to be procured. If no procurement specification is used enter "Commercial". Attach one copy of applicable documents for review.

Block 11 - Enter the screening specification and appropriate revision letter to which the part or device is to be tested. Attach one copy of applicable documents for review.

Block 12 - Describe the critical parameters that dictate the use of this part.

Block 13 - Enter the basis for justification for the usage of the part. Indicate the qualification status of the part. The criterion for qualification by similarity includes similarity of design and function and includes fabrication by same manufacturer using the same process and quality controls as the standard part. If prior usage on NASA spacecraft is used as basis for acceptance, indicate the programs where used with launch dates and orbital life. The part application must be congruent with that used in prior programs. Attach on copy of the qualification test plan to be used if none of the above is applicable.

Block 14 - For PAB Request generated by the Engineer, enter the signature and title of the preparer, the parts/reliability engineer and the project program engineer or his/her designated representative. The signatures provide that appropriate personnel have reviewed the request and that the information included is accurate and complete.